

54AC/74AC373 • 54ACT/74ACT373

Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

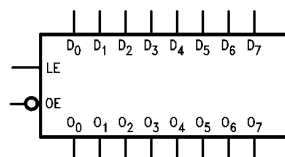
- I_{CC} and I_{OZ} reduced by 50%
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC373: 5962-87555
 - 'ACT373: 5962-87556

Commercial	Military	Package Number	Package Description
74ACT373PC		N20A	20-Lead Molded Dual-In-Line (0.300" Wide)
74ACT373SC (Note 1)		M20B	20-Lead Molded Small Outline (0.300" Wide), JEDEC
74ACT373SJ (Note 1)		M20D	20-Lead Molded Small Outline, EIAJ Type II
74ACT373MTC (Note 1)		MTC20	20-Lead Molded Thin Shrink Small Outline Package, JEDEC
74ACT373MSA (Note 1)		MSA20	20-Lead Molded Small Shrink Outline Package, (EIAJ SSOP)
	54ACT373DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
	54ACT373FM (Note 2)	W20A	20-Lead Cerpak

Note 1: Devices also available in 13" Tape and Reel. Use suffix SCX, SJX, and MTCX.

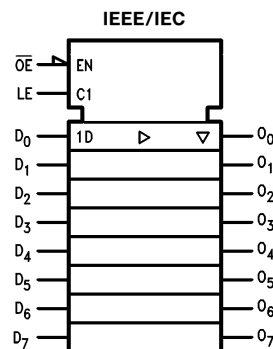
Note 2: Military grade device with environmental and burn-in processing, use suffix DMQB, FMQB and LMQB.

Logic Symbols



TL/F/9958-1

Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O ₀ –O ₇	TRI-STATE Latch Outputs

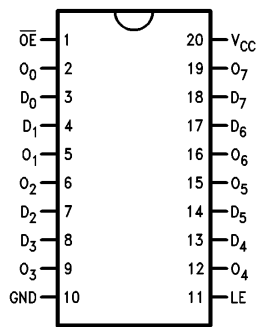


TL/F/9958-2

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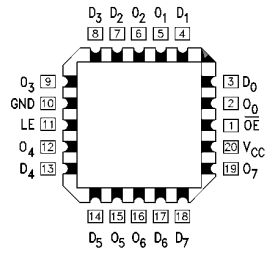
Connection Diagrams

Pin Assignment for DIP, Flatpak, SSOP, SOIC and TSSOP



TL/F/9958-3

Pin Assignment for LCC



TL/F/9958-4

Functional Description

The 'AC/ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level

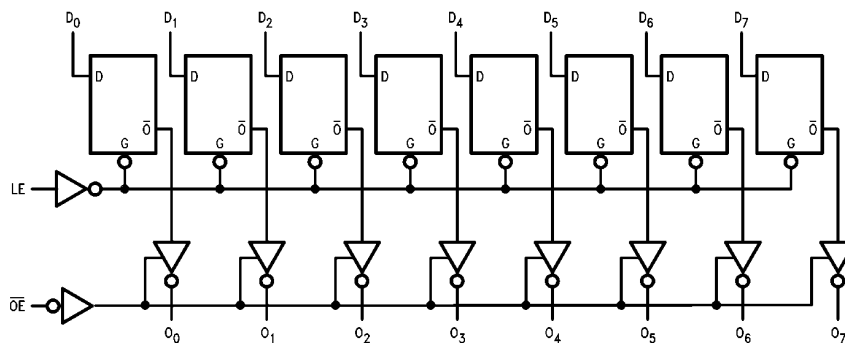
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/9958-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	−20 mA
$V_I = -0.5V$	+20 mA
$V_I = V_{CC} + 0.5V$	
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	−20 mA
$V_O = -0.5V$	+20 mA
$V_O = V_{CC} + 0.5V$	
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	2.1 3.15 3.85		V	V _{OUT} = 0.1V or V _{CC} − 0.1V	
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	0.9 1.35 1.65		V	V _{OUT} = 0.1V or V _{CC} − 0.1V	
V _{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	2.9 4.4 5.4		V	I _{OUT} = −50 μA	
		3.0 4.5 5.5		2.56 3.86 4.86	2.4 3.7 4.7	2.46 3.76 4.76		V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA	
		3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1		V	I _{OUT} = 50 μA	
	3.0 4.5 5.5		0.36 0.36 0.36	0.50 0.50 0.50	0.44 0.44 0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA		
	I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0		μA	V _I = V _{CC} , GND

*All outputs loaded, thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OZ}	Maximum TRI-STATE Current	5.5		± 0.25	± 5.0		± 2.5		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50		−75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0		μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
		5.5		4.86	4.70	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5		0.36	0.50	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Current	5.5		±0.25	±5.0	±2.5	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	mA	V _I = V _{CC} − 2.1V
I _{OLD}	†Minimum Dynamic	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current	5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = +25°C C _L = 50 pF			T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	10.0 7.0	13.5 9.5	1.0 1.5	16.5 11.5	1.5 1.5	15.0 10.5	ns
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	9.5 7.0	13.0 9.5	1.0 1.5	16.0 11.5	1.5 1.5	14.5 10.5	ns
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	10.0 7.5	13.5 9.5	1.0 1.5	16.5 12.0	1.5 1.5	15.0 10.5	ns
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	9.5 7.0	12.5 9.5	1.0 1.5	15.0 11.0	1.5 1.5	14.0 10.5	ns
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	9.0 7.0	11.5 8.5	1.0 1.5	14.0 10.5	1.0 1.0	13.0 9.5	ns
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	8.5 6.5	11.5 8.5	1.0 1.5	13.5 10.0	1.0 1.0	13.0 9.5	ns
t _{PHZ}	Output Disable Time	3.3 5.0	1.5 1.5	10.0 8.0	12.5 11.0	1.0 1.5	16.0 13.5	1.0 1.0	14.5 12.5	ns
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	8.0 6.5	11.5 8.5	1.0 1.5	13.0 10.5	1.0 1.0	12.5 10.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		54AC	74AC	Units
			T _A = +25°C C _L = 50 pF		T _A = −55°C to +125°C C _L = 50 pF	T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0	3.5 2.0	5.5 4.0	6.5 5.0	6.0 4.5	ns
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0	−3.0 −1.5	1.0 1.0	1.0 1.0	1.0 1.0	ns
t _w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.0	5.5 4.0	6.5 5.0	6.0 4.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.5	8.5	10.0	1.5	12.5	1.5	11.5	ns
t _{PHL}	Propagation Delay D _n to O _n	5.0	2.0	8.0	10.0	1.5	12.5	1.5	11.5	ns
t _{PLH}	Propagation Delay LE to O _n	5.0	2.5	8.5	11.0	1.5	12.5	2.0	11.5	ns
t _{PHL}	Propagation Delay LE to O _n	5.0	2.0	8.0	10.0	1.5	11.5	1.5	11.5	ns
t _{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.5	11.5	1.5	10.5	ns
t _{PZL}	Output Enable Time	5.0	2.0	7.5	9.0	1.5	11.0	1.5	10.5	ns
t _{PHZ}	Output Disable Time	5.0	2.5	9.0	11.0	1.5	14.0	2.5	12.5	ns
t _{PLZ}	Output Disable Time	5.0	1.5	7.5	8.5	1.5	11.0	1.0	10.0	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74ACT		54ACT	74ACT	Units
			T _A = +25°C C _L = 50 pF		T _A = −55°C to +125°C C _L = 50 pF	T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	0.8	2.5	8.5	3.5	ns
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	0	0	1.0	1.0	ns
t _w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.5	8.0	ns

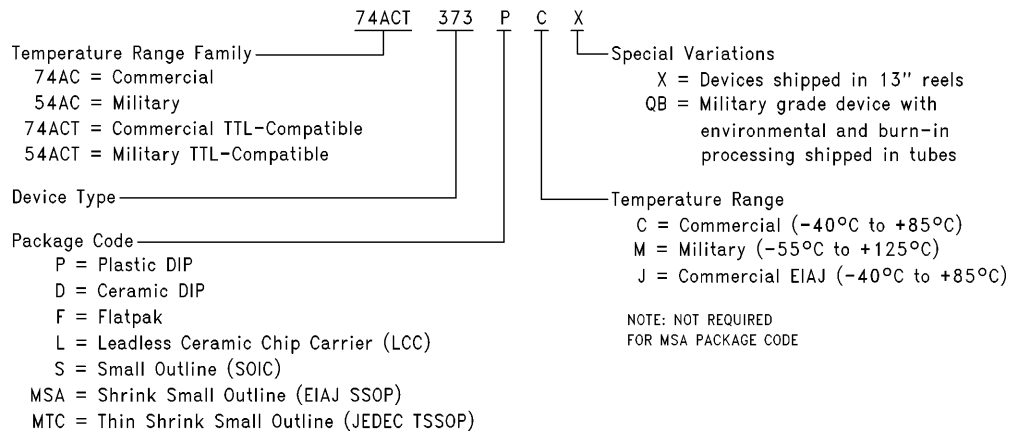
*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	40.0	pF	V _{CC} = 5.0V

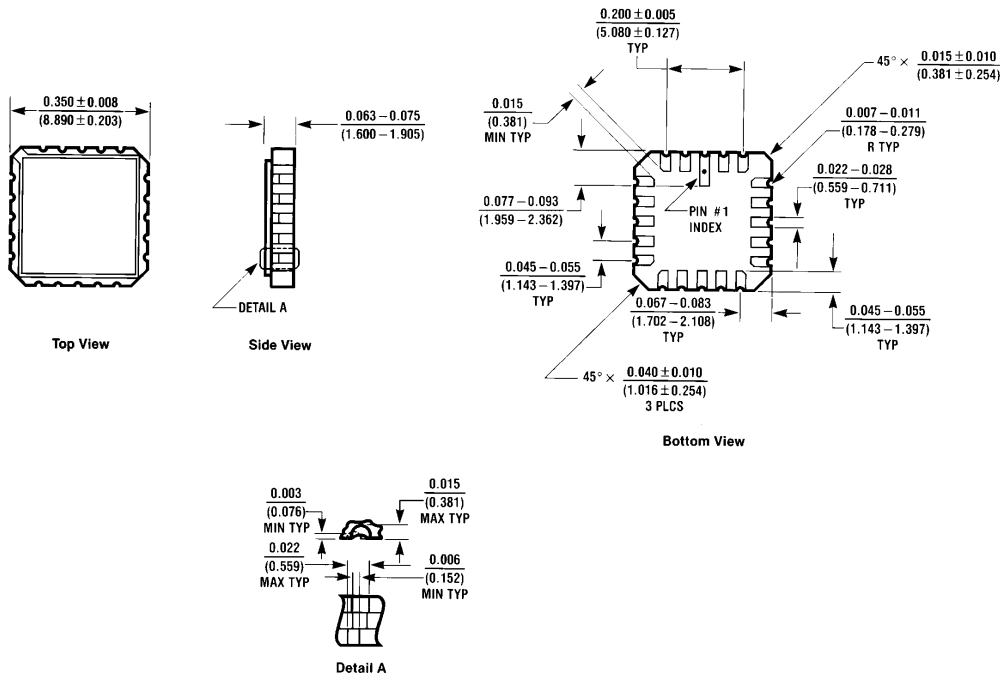
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



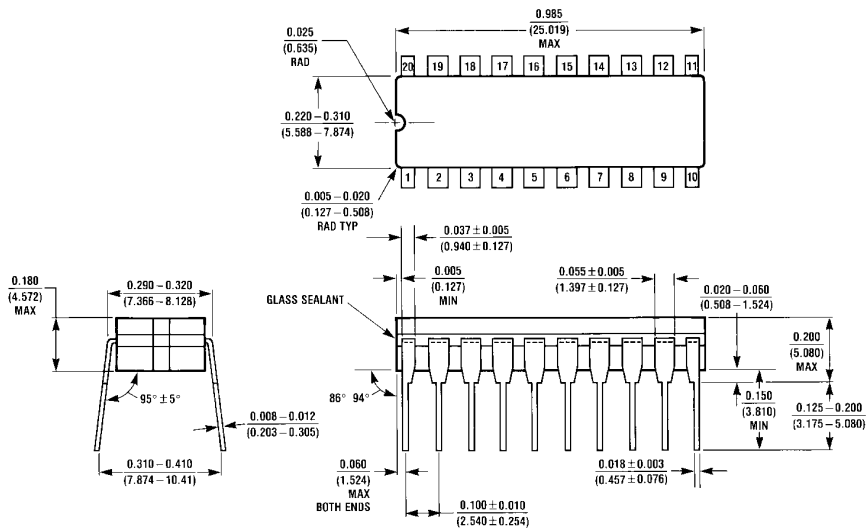
TL/F/9958-7

Physical Dimensions inches (millimeters) unless otherwise noted



20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

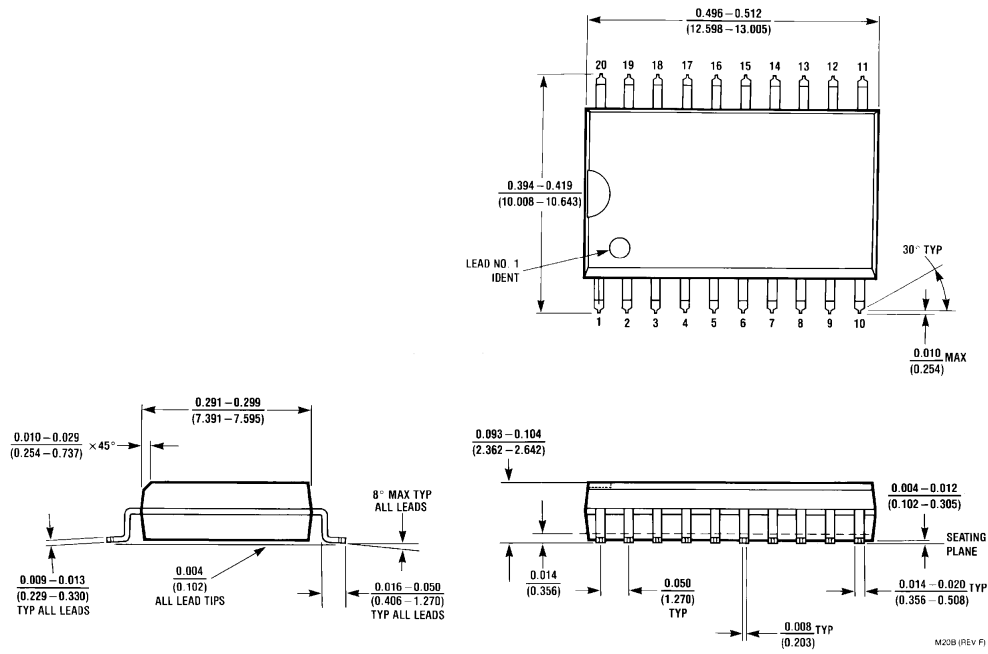
E20A (REV D)



20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

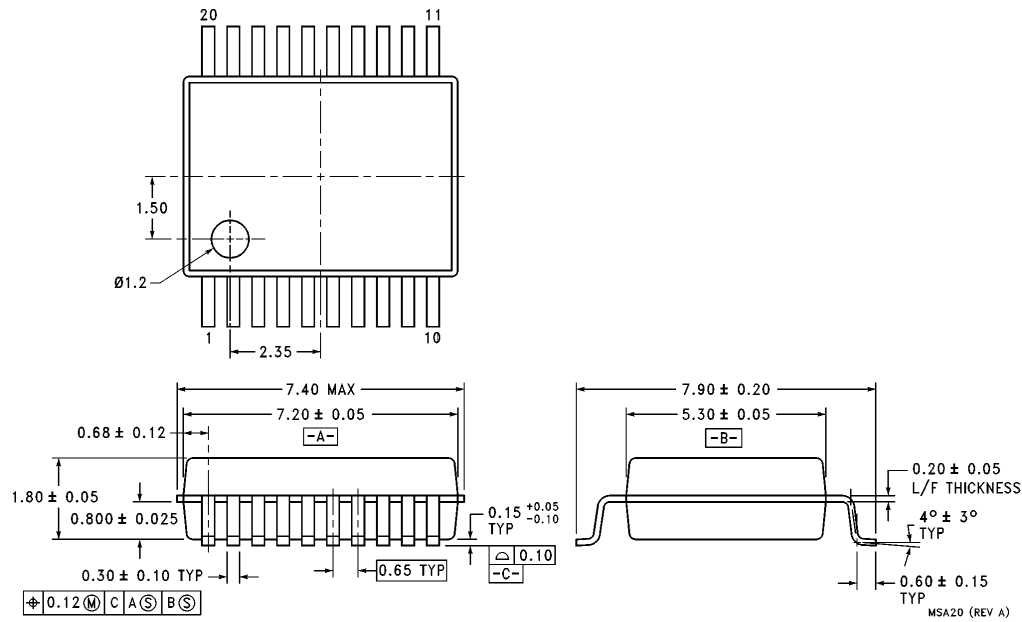
J20A (REV M)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



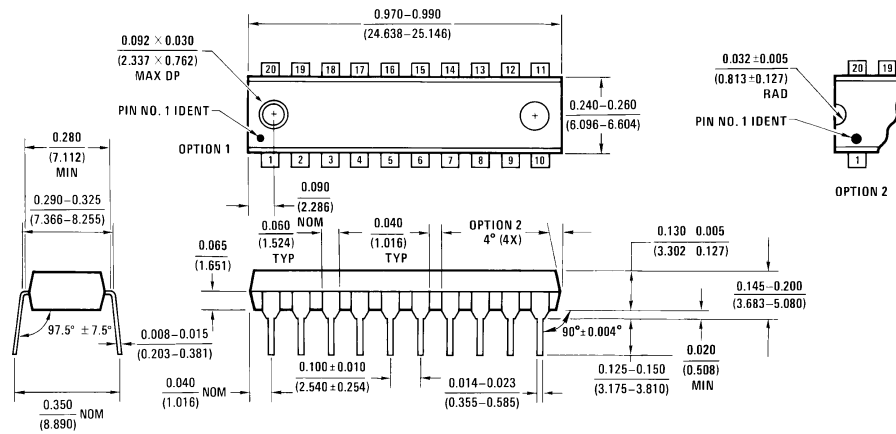
**20 Lead Small Outline Integrated Circuit (S)
NS Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



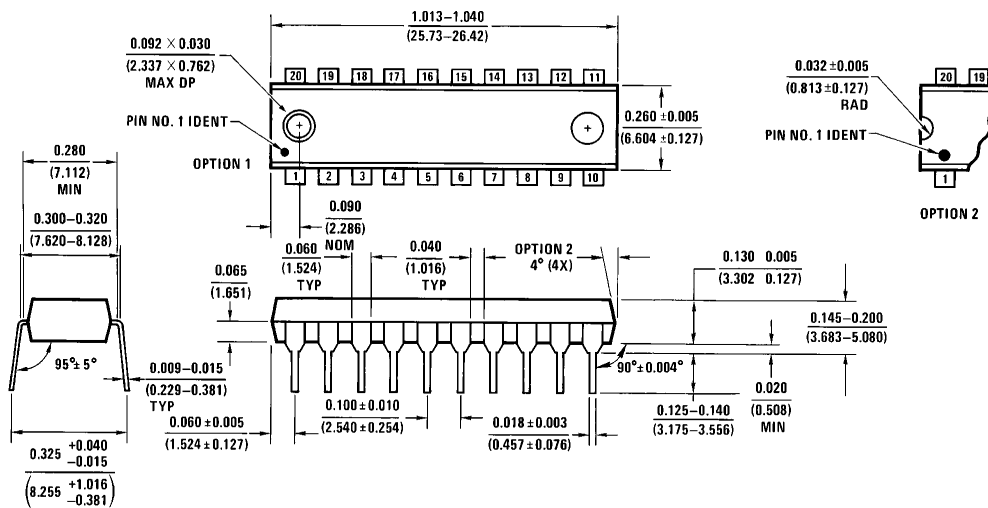
20 Lead Plastic EIAJ SSOP (MSA)
NS Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20B (REV A)

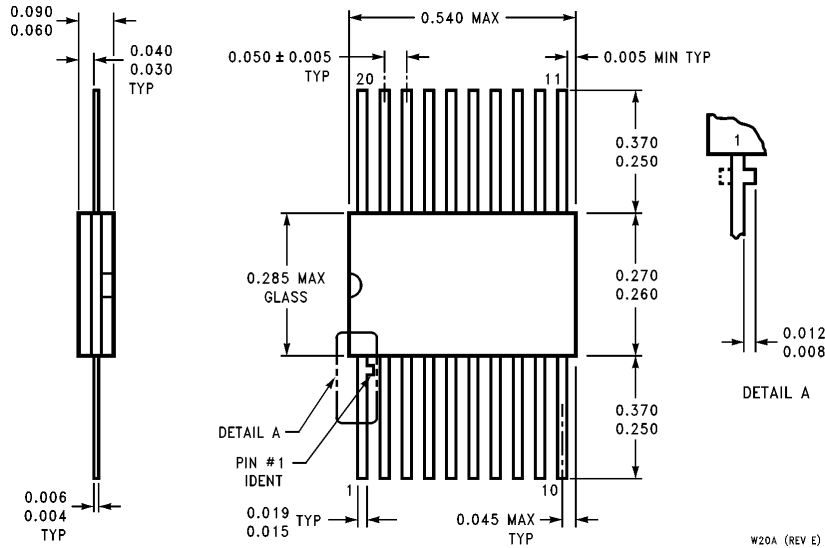
**20-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC20**



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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