

IR2136/IR21362/IR21363 (J&S)

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V (IR2136/
IR21363) or 12 to 20V (IR21362)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Lowside outputs out of phase with inputs. High
side outputs out of phase (IR2136/IR21363) or in
phase (IR21362) with inputs.
- Cross-conduction prevention logic
- 3.3V logic compatible
- Lower di/dt gate driver for better noise immunity
- Externally programmable delay for automatic fault
clear

Description

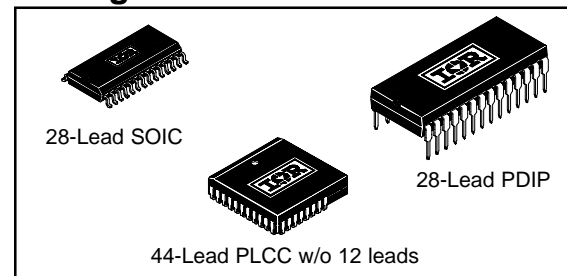
The IR2136/IR21362/IR21363(J&S) are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared

3-PHASE BRIDGE DRIVER

Product Summary

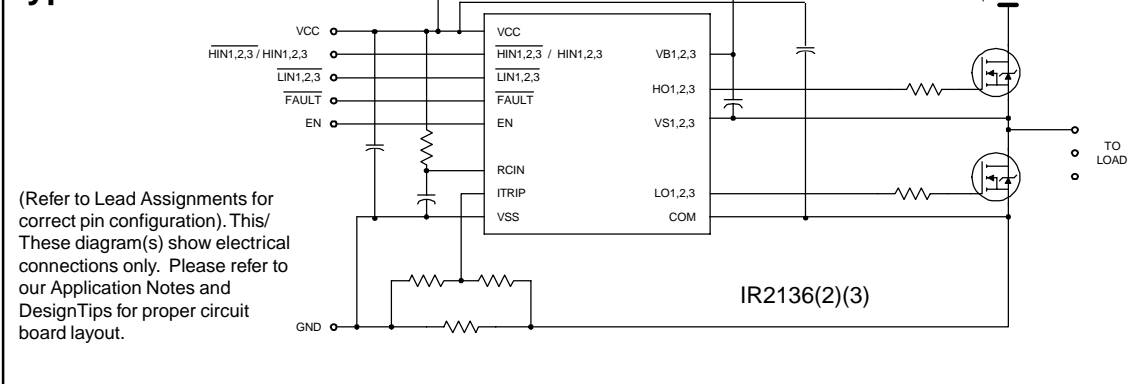
V_{OFFSET}	600V max.
$I_{\text{O}+/-}$	120 mA / 250 mA
V_{OUT}	10 - 20V or 12V - 20V
Deadtime (typ.)	200 nsec
$t_{\text{on/off}}$ (typ.)	400 nsec

Packages



automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.

Typical Connection



IR2136/IR21362/IR21363(J&S)

International
IR Rectifier

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	High side offset voltage	-0.3	600	V	
V _{BS}	High side floating supply voltage	-0.3	25		
V _{HO}	High side floating output voltage	V _{S1,2,3} - 0.3	V _{B1,2,3} + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{SS}	Logic ground	V _{CC} - 25	V _{CC} + 0.3		
V _{LO1,2,3}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Input voltage $\overline{\text{LIN}}$, $\overline{\text{HIN}}$ (IR2136/IR21363), $\overline{\text{HIN}}$ (IR21362) ITRIP, EN, RCIN	V _{SS} - 0.3	V _{SS} + 15		
V _{FLT}	FAULT output voltage	V _{SS} - 0.3	V _{CC} + 0.3		
dV/dt	Allowable offset voltage slew rate	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
R _{thJA}	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T _J	Junction temperature	—	125	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _{B1,2,3}	High side floating supply voltage	V _{S1,2,3} + 10	V _{S1,2,3} + 20	V
V _{S1,2,3}	High side floating supply offset voltage	Note 1	600	
V _{HO1,2,3}	High side output voltage	V _{S1,2,3}	V _{B1,2,3}	
V _{LO1,2,3}	Low side output voltage	0	V _{CC}	
V _{CC}	Low side and logic fixed supply voltage	10	20	
V _{SS}	Logic ground	-5	5	
V _{FLT}	$\overline{\text{FAULT}}$ output voltage	V _{SS}	V _{CC}	
V _{RCIN}	RCIN input voltage	V _{SS}	V _{CC}	
V _{ITRIP}	ITRIP input voltage	V _{SS}	V _{SS} + 5	
V _{IN}	Logic input voltage $\overline{\text{LIN}}$, $\overline{\text{HIN}}$ (IR2136), $\overline{\text{HIN}}$ (IR21362), EN	V _{SS}	V _{SS} + 5	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V. Logic state held for V_S of COM -5V to -COM -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ and $L_{S1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "1" input voltage $\overline{HIN1,2,3}$	3	—	—	V		
V_{IL}	Logic "1" input voltage $\overline{LIN1,2,3}$, $\overline{HIN1,2,3}$ Logic "0" input voltage $\overline{HIN1,2,3}$	—	—	0.8			
$V_{EN,TH+}$	EN positive going threshold	—	—	3			
$V_{EN,TH-}$	EN negative going threshold	0.8	—	—	mV		
$V_{IT,TH+}$	ITRIP positive going threshold	370	460	550			
$V_{IT,HYS}$	ITRIP input hysteresis	—	70	—			
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—			
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—			
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20\text{ mA}$	
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20\text{ mA}$	
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	IR2136	8.0	8.9	9.8	V	
		IR21362	9.6	10.4	11.2		
		IR21363	10.7	11.2	11.7		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	IR2136	7.4	8.2	9.0		
		IR21362	8.6	9.4	10.2		
		IR21363	10.5	11.0	11.5		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lockout hysteresis	IR2136	0.3	0.7	—		
		IR21362	0.5	1.0	—		
		IR21363	—	0.2	—		
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_{B1,2,3} = V_{S1,2,3} = 600\text{V}$	
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		$V_{IN} = 0\text{V or } 5\text{V}$	
I_{QCC}	Quiescent V_{CC} supply current	—	1	2	mA		
$V_{IN, CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.9	5.2	5.5	V	$I_{IN} = 100\mu\text{A}$	
I_{LIN+}	Input bias current (LOUT = HI)	—	150	400	μA	$V_{LIN} = 0\text{V}$	
I_{LIN-}	Input bias current (LOUT = LO)	—	100	250		$V_{LIN} = 5\text{V}$	
I_{HIN+}	Input bias current (HOUT = HI)	IR2136(3)	—	150		300	$V_{HIN} = 0\text{V}$
		IR21362	—	—		100	$V_{HIN} = 5\text{V}$
I_{HIN-}	Input bias current (HOUT = LO)	IR2136(3)	—	100		250	$V_{HIN} = 5\text{V}$
		IR21362	—	0		1	$V_{HIN} = 0\text{V}$
I_{ITRIP+}	"high" ITRIP input bias current	—	—	100			$V_{ITRIP} = 5\text{V}$
I_{ITRIP-}	"low" ITRIP input bias current	—	0	1			$V_{ITRIP} = 0\text{V}$

Static Electrical Characteristics cont.

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ and $L_{S1,2,3}$). The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{EN+}	"high" ENABLE input bias current	—	—	100	μA	$V_{ENABLE} = 5V$
I_{EN-}	"low" ENABLE input bias current	—	0	1		$V_{ENABLE} = 0V$
I_{RCIN}	RCIN input bias current	—	0	1		$V_{RCIN} = 0V$ or $15V$
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, $PW \leq 10 \mu s$
$R_{ON,RCIN}$	RCIN low on resistance	—	60	—	Ω	
$R_{ON,FLT}$	FAULT low on resistance	—	60	—		

Dynamic Electrical Characteristics

$V_{CC} = V_{BS} = V_{BIAS} = 15V$, $V_{S1,2,3} = V_{SS} = COM$, $T_A = 25^\circ C$ and $C_L = 1000 pF$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	400	—	nS	$V_{IN} = 0$ & $5V$ $V_{S1,2,3} = 0$ to $600V$
t_{off}	Turn-off propagation delay	—	380	—		
t_r	Turn-on rise time	—	110	—		
t_f	Turn-off fall time	—	50	—		
t_{EN}	ENABLE low to output shutdown propagation delay	—	400	—		$V_{IN}, V_{EN} = 0V$ or $5V$
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	700	—		$V_{ITRIP} = 5V$
t_{bl}	ITRIP blanking time	100	150	—		$V_{IN} = 0V$ or $5V$ $V_{ITRIP} = 5V$
t_{FLT}	ITRIP to FAULT propagation delay	—	500	—		$V_{IN} = 0V$ or $5V$ $V_{ITRIP} = 5V$
t_{FILIN}	Input filter time (H_{IN} , L_{IN} , EN)	100	200	—	$V_{IN} = 0$ & $5V$	
t_{FLTCLR}	FAULT clear time RCIN: $R=2meg$, $C=1nF$	—	1.8	—	mS	$V_{IN} = 0V$ or $5V$ $V_{ITRIP} = 0V$
DT	Deadtime	—	250	—	nS	$V_{IN} = 0$ & $5V$
MT	Matching delay ON and OFF	—	0	80		
MDT	Matching delay, max (t_{on}, t_{off}) - min (t_{on}, t_{off}), (t_{on}, t_{off} are applicable to all 3 channels)	—	0	75		External dead time >400nsec
PM	Output pulse width matching, $PW_{in} - PW_{out}$ (fig.2)	—	0	75		

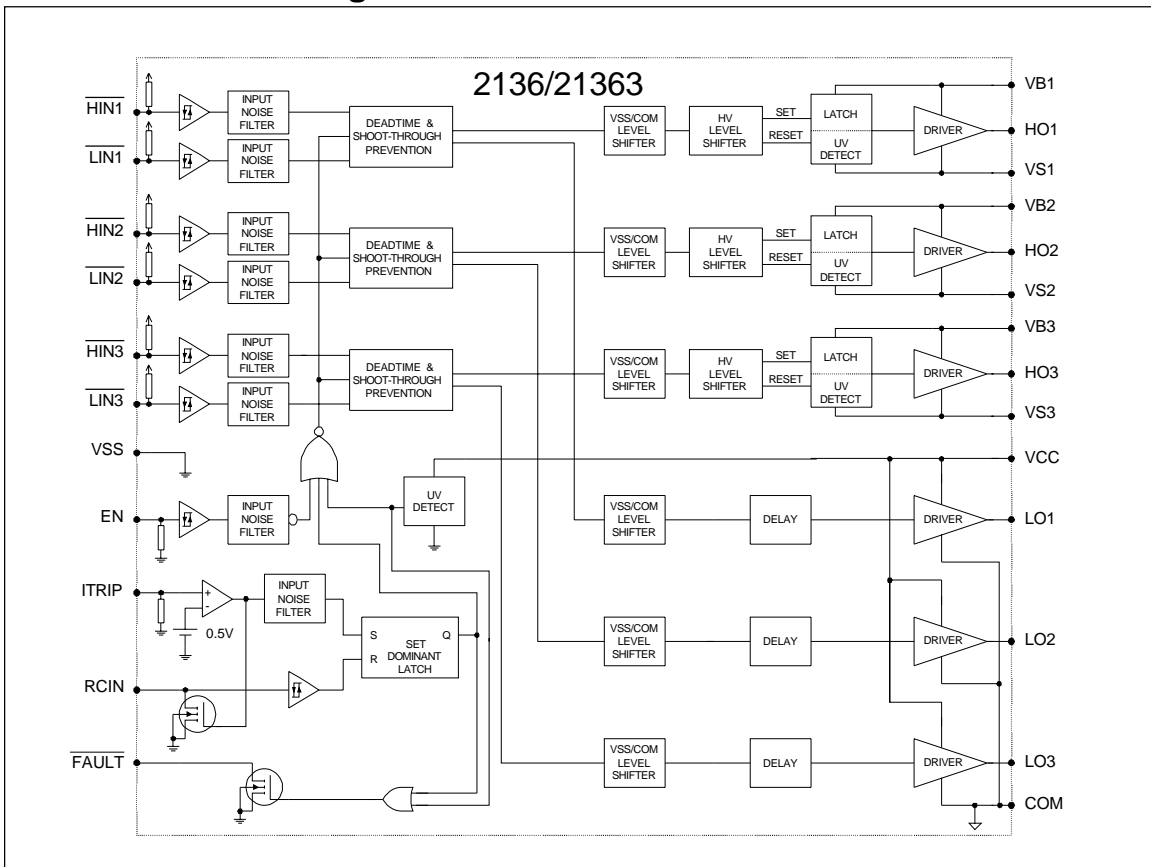
NOTE: For high side PWM, H_{IN} pulse width must be $\geq 1\mu sec$

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VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	LIN1,2,3	0
15V	15V	0V	5V	high imp	LIN1,2,3	HIN1,2,3
15V	15V	>VITRIP	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

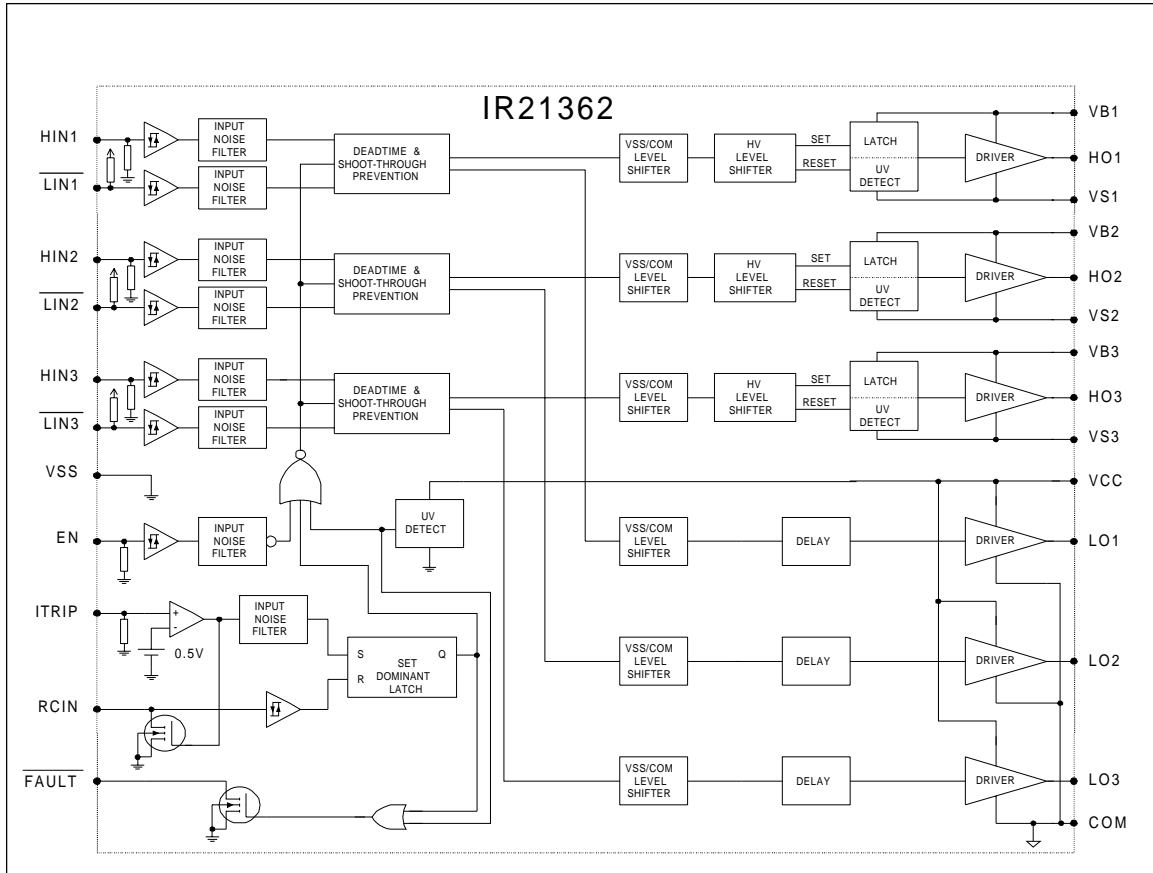
Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
Note 1: UVCC is not latched, when VCC>UVCC, FAULT returns to high impedance.
Note 2: When ITRIP < VITRIP, FAULT returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

Functional Block Diagram



IR2136/IR21362/IR21363(J&S)

Functional Block Diagram



Lead Definitions

Symbol	Description
VCC	Low side and logic fixed supply
VSS	Logic Ground
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase (IR2136/IR21363)
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362)
LIN1,2,3	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR} , then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR} , approximately equal to $R \cdot C$. When $RCIN > 8V$, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
VB1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
VS1,2,3	High voltage floating supply returns
LO1,2,3	Low side gate driver output

Lead Assignments

<p>28 Lead PDIP</p>	<p>44 Lead PLCC w/o 12 leads</p>	<p>28 lead SOIC (wide body)</p>
IR2136/IR21363	IR2136J/IR21363J	IR2136S/IR21363S

IR2136/IR21362/IR21363(J&S)

International
IR Rectifier

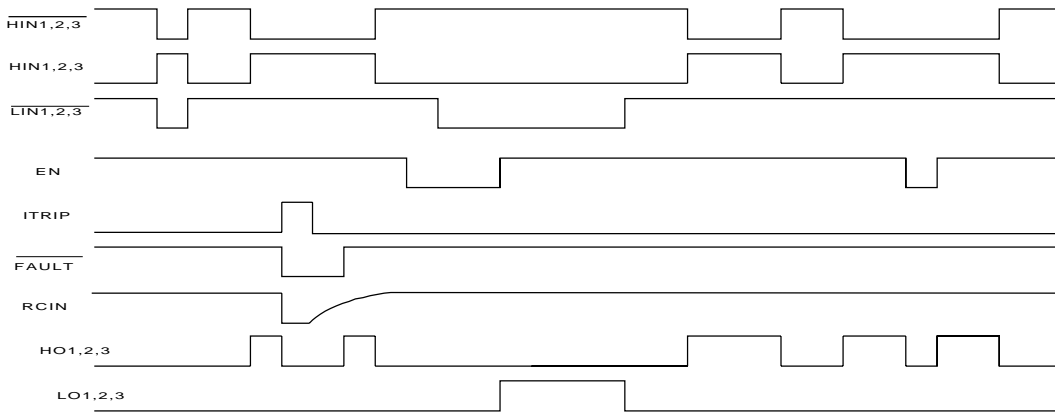
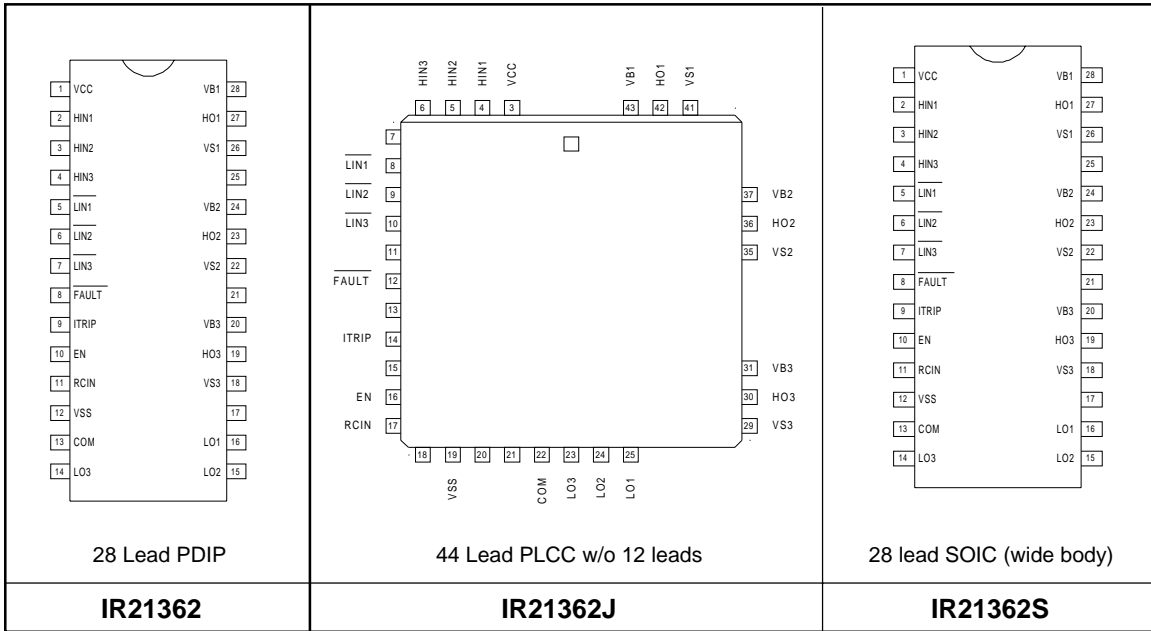


Figure 1. Input/Output Timing Diagram

IR2136/IR21362/IR21363(J&S)

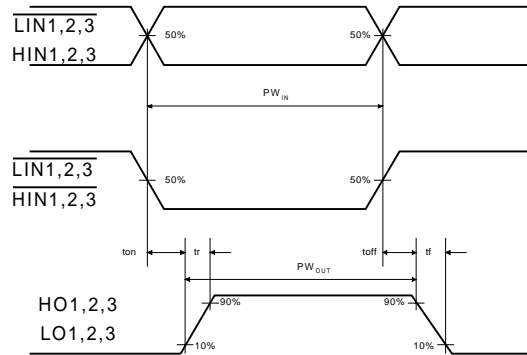


Figure 2. Switching Time Waveforms

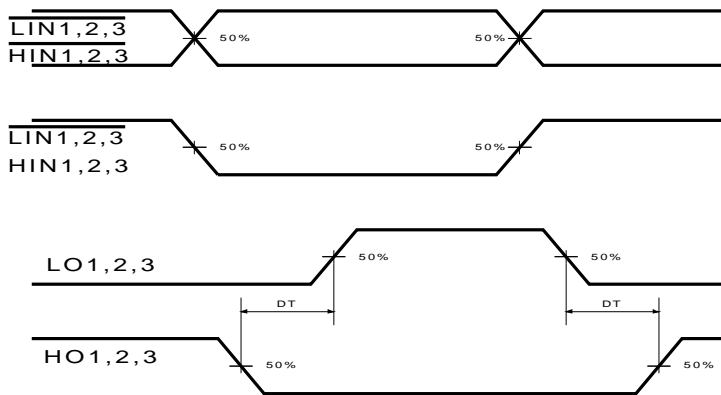


Figure 3. Internal Deadtime Timing Waveforms

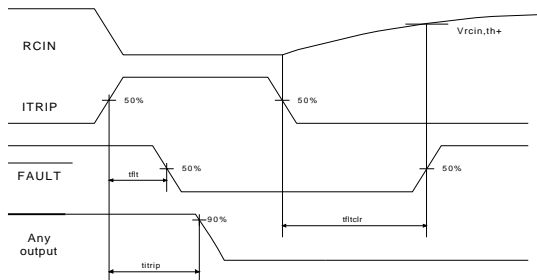


Figure 4. ITRIP/RCIN Timing Waveforms

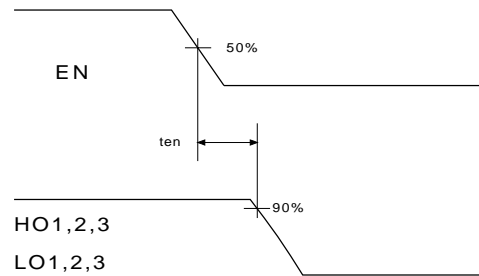
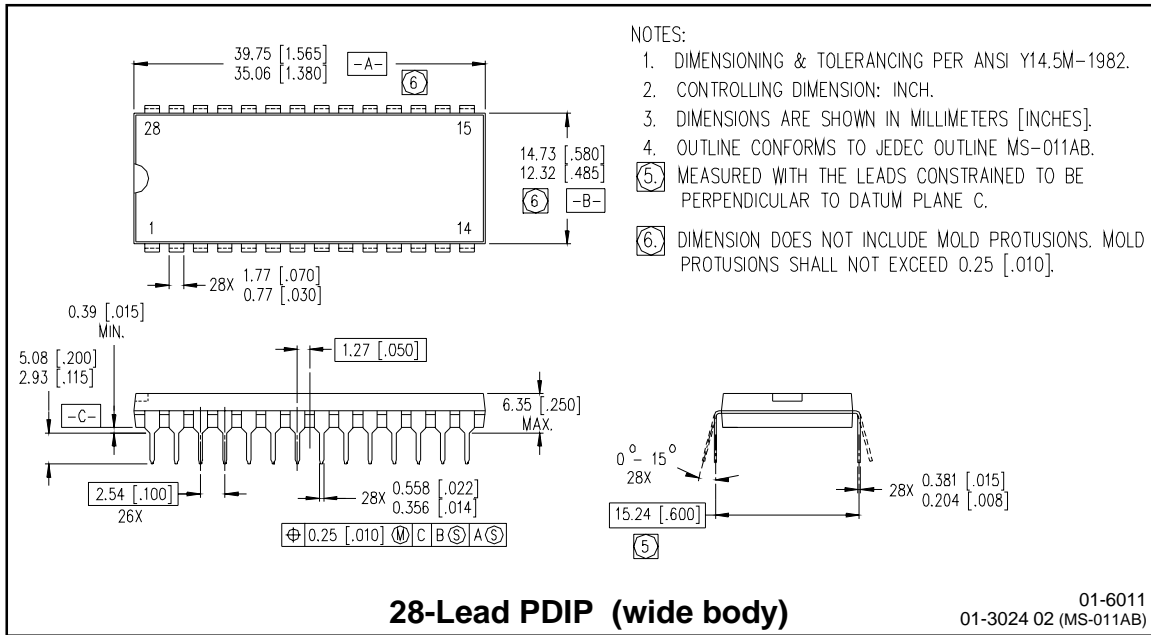


Figure 5. Output Enable Timing Waveform

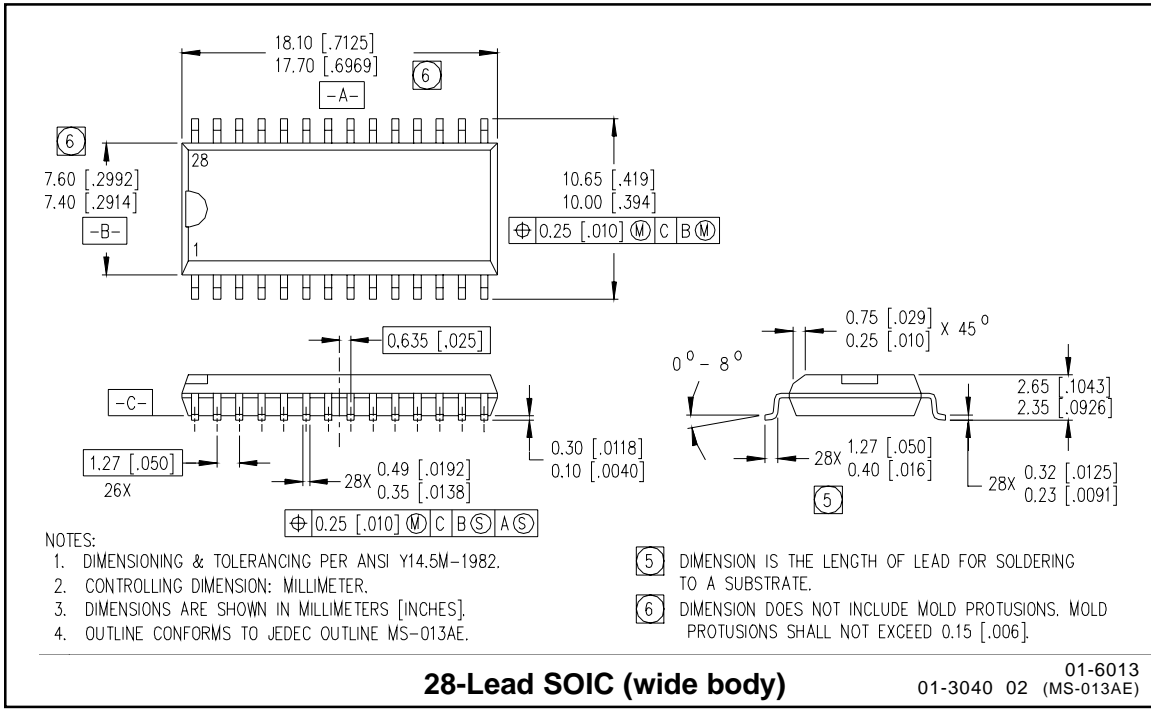
IR2136/IR21362/IR21363(J&S)

International
IR Rectifier

Case outlines



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
 - ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
 - ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.
 - ⑤ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
 - ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

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