FAIRCHILD SEMICONDUCTOR®

January 2009

MM74HC174 — Hex D-Type Flip-Flops with Clear

Features

- Typical Propagation Delay: 16ns
- Wide Operating Voltage Range: 2V–6V
- Low Input Current: 1µA maximum
- Low Quiescent Current: 80µA (74HC Series)
- Output Drive: 10 LSTTL Loads

Description

The MM74HC174 edge-triggered flip-flops utilize silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low-power, and speeds comparable to low-power Schottky TTL circuits. This device contains six master-slave flip-flops with a common clock and common clear. Data on the D input with the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. When LOW, the input sets all outputs to a LOW state.

Each output can drive ten low-power Schottky TTL equivalent loads. The MM74HC174 is functionally and pin comparable to the 74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
MM74HC174M	-40 to +85°C	RoHS	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Inch Narrow	Tubes
MM74HC174MX	-40 to +85°C			Tape and Reel
MM74HC174MTC	-40 to +85°C	RoHS	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tubes
MM74HC174MTCX	-40 to +85°C			Tape and Reel
MM74HC174N	-40 to +85°C	RoHS	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Inch Wide	Tubes

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Pin Configuration

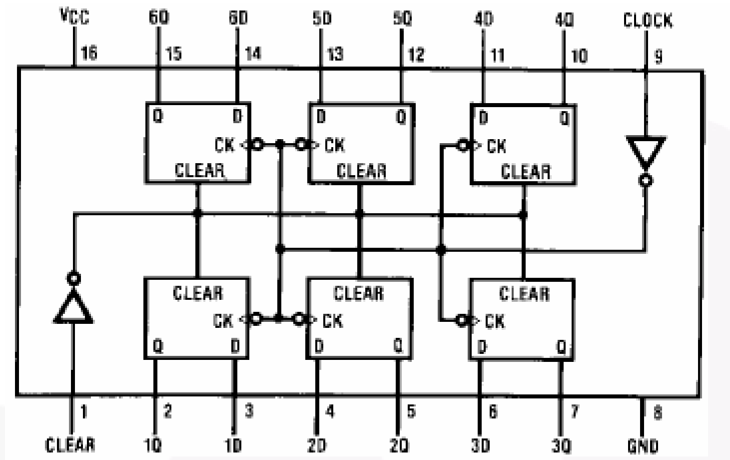

Figure 1. Pin Configuration (Top View)

Truth Table (Each Flip-Flop)

Inputs			Output
Clear	**Clock**	**D**	**Q**
LOW	Don't Care	Don't Care	LOW
HIGH	↑(1)	HIGH	HIGH
HIGH	↑(1)	LOW	LOW
HIGH	LOW	Don't Care	Q_0(2)

Notes:
1. Transition from LOW to HIGH level.
2. The level of Q before the indicated steady-state input conditions were established.

Logic Diagram

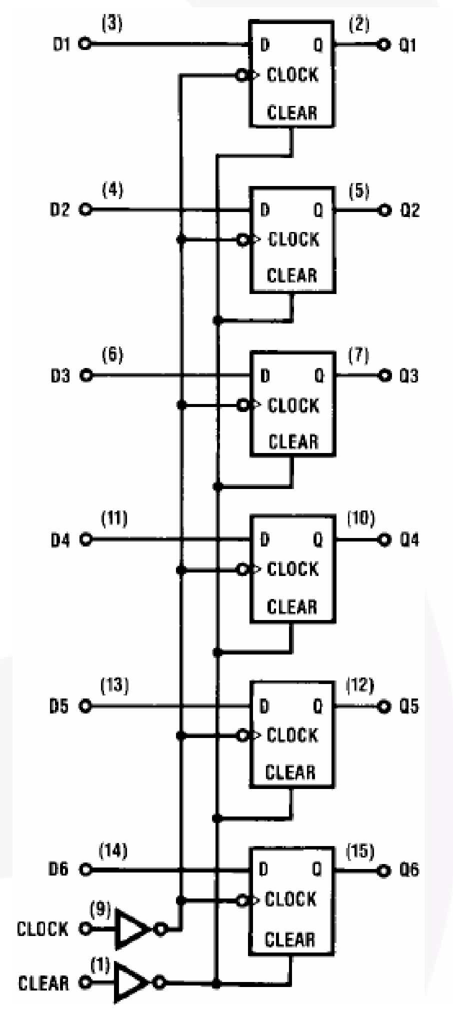

Figure 2. Logic Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Unless otherwise noted, all voltages are referenced to ground.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	+7.0	V
V_{IN}	DC Input Voltage		-1.5 to V_{CC}	+1.5	V
V_{OUT}	DC Output Voltage		-0.5 to V_{CC}	+0.5	V
I_{IK}, I_{OK}	Clamp Diode Current			±20	mA
I_{OUT}	DC Output Current, per Pin			±25	mA
I_{CC}	DC V_{CC} or GND Current, per Pin			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
P_D	Power Dissipation(3)	TSSOP, PDIP		600	mW
		SOIC		500	
T_L	Lead Temperature, Soldering10 Seconds			260	°C

Notes:
3. Power dissipation temperature derating— plastic "N" package:12mW/°C from 65° to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		-40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC}=2.0V		1000	ns
		V_{CC}=4.5V		500	ns
		V_{CC}=6.0V		400	ns

DC Electrical Characteristics[4]

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=25°C		T_A=-40 to+85°C	T_A=-55 to +125°C	Units
				Typ.	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input		2.0		1.5	1.5	1.5	V
			4.5		3.15	3.15	3.15	
			6.0		4.2	4.2	4.2	
V_{IL}	Minimum LOW Level Input		2.0		0.5	0.5	0.5	V
			4.5		1.35	1.35	1.35	
			6.0		1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq 20\mu A$	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
			6.0	6.0	5.9	5.9	5.9	
		$V_{IN}=V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq 4.0mA$	4.5	4.20	3.98	3.84	3.70	
		$V_{IN}=V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq 5.2mA$	6.0	5.70	5.48	5.34	5.20	
V_{OL}	Minimum LOW Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq 20\mu A$	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
			6.0	0	0.1	0.1	0.1	
		$V_{IN}=V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq 4.0mA$	4.5	00.2	0.26	0.33	0.40	
		$V_{IN}=V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq 5.2mA$	6.0	0.20	0.26	0.33	0.40	
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0\mu A$	6.0		8	80	160	µA

Note:

4. For a power supply of 5V ±10%, the worst-case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. The 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V, respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occurs for CMOS at the higher voltage, so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C and C_L = 15pF, t_r = t_f = 6ns.

Symbol	Parameter	Typ.	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency	50	30	MHz
t_{PHL},t_{PLH}	Maximum Propagation Delay, Clock, or Clear to Output	16	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock	-2	5	ns
t_S	Minimum Setup Time, Data to Clock	10	20	ns
t_H	Minimum Hold Time, Clock to Data	0	5	ns
t_W	Minimum Pulsewidth, Clock or Clear	10	16	ns

AC Electrical Characteristics(5)

C_L = 50pF, t_r = t_f = 6ns unless otherwise noted.

Symbol	Parameter	V_{CC} (V)	T_A=25°C		T_A=-40 to+85°C	T_A=-55 to +125°C	Units
			Typ.	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	2.0		5	4	3	MHz
		4.5		27	21	18	
		6.0		31	24	20	
t_{PHL},t_{PLH}	Maximum Propagation Delay, Clock, or Clear to Output	2.0	55	165	206	248	ns
		4.5	18	33	41	49	
		6.0	16	28	35	42	
t_{REM}	Minimum Setup Time, Data to Clock	2.0	1	5	5	5	ns
		4.5	1	5	5	5	
		6.0	1	5	5	5	
t_S	Minimum Setup Time, Data to Clock	2.0	42	100	125	150	ns
		4.5	12	20	25	30	
		6.0	10	17	21	25	
t_H	Minimum Hold Time, Clock to Data	2.0	1	5	5	5	ns
		4.5	1	5	5	5	
		6.0	1	5	5	5	
t_W	Minimum Pulse Width, Clock or Clear	2.0	35	80	106	120	ns
		4.5	10	16	20	24	
		6.0	8	14	18	20	
t_{TLH},t_{THL}	Maximum Output Rise and Fall Time	2.0	30	75	95	110	ns
		4.5	8	15	19	22	
		6.0	7	13	16	19	
t_r,t_f	Maximum Input Rise and Fall Time	2.0		1000	1000	1000	ns
		4.5		500	500	500	
		6.0		400	400	400	
C_{PD}	Power Dissipation Capacitance(5) (per Package)		136				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note:

5. C_{PD} determines the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no-load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Waveforms

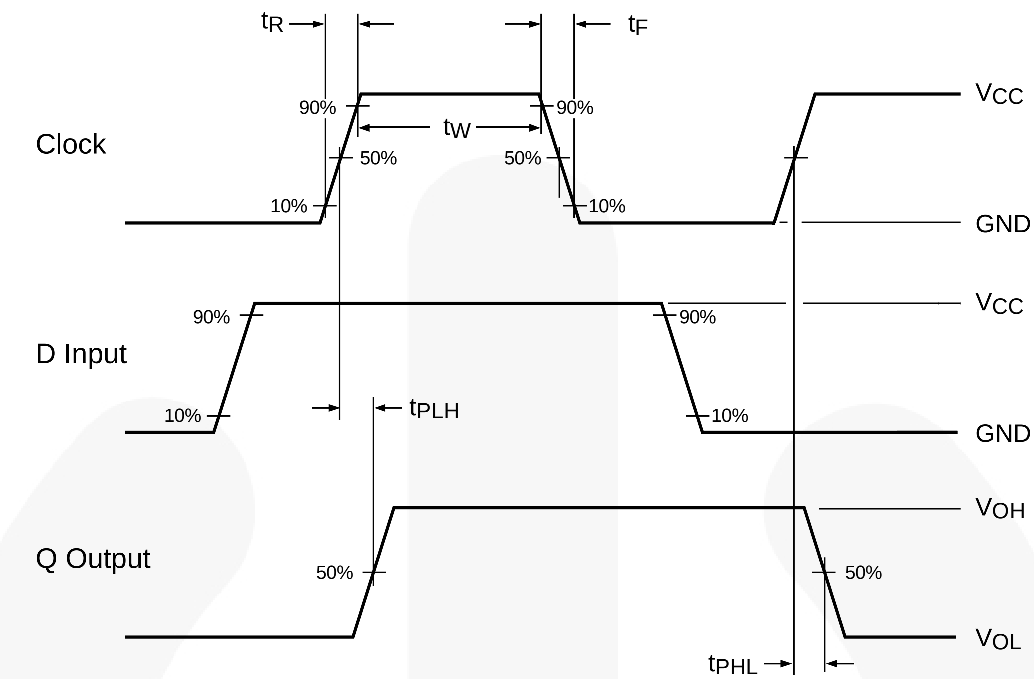

Figure 3. AC Waveform

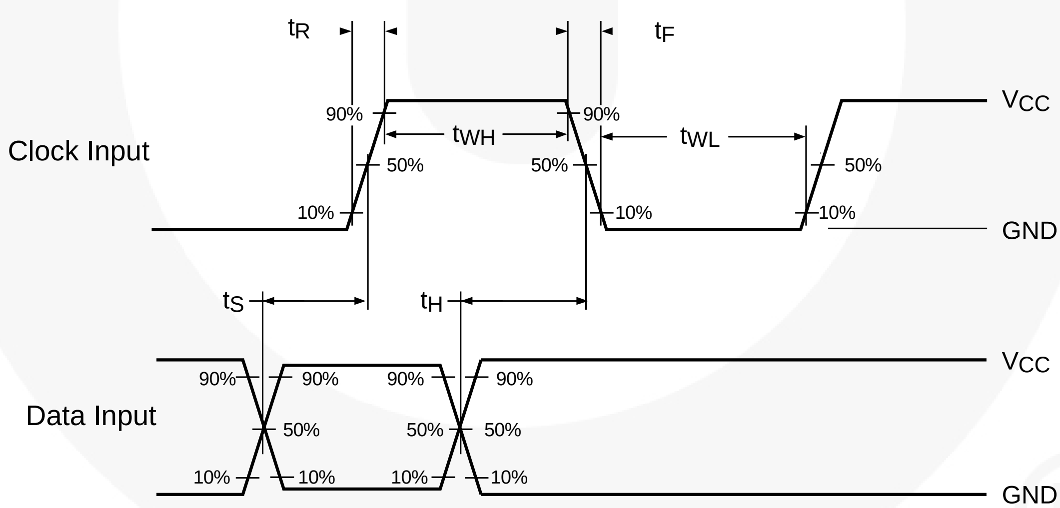

Figure 4. AC Waveform

Physical Dimensions

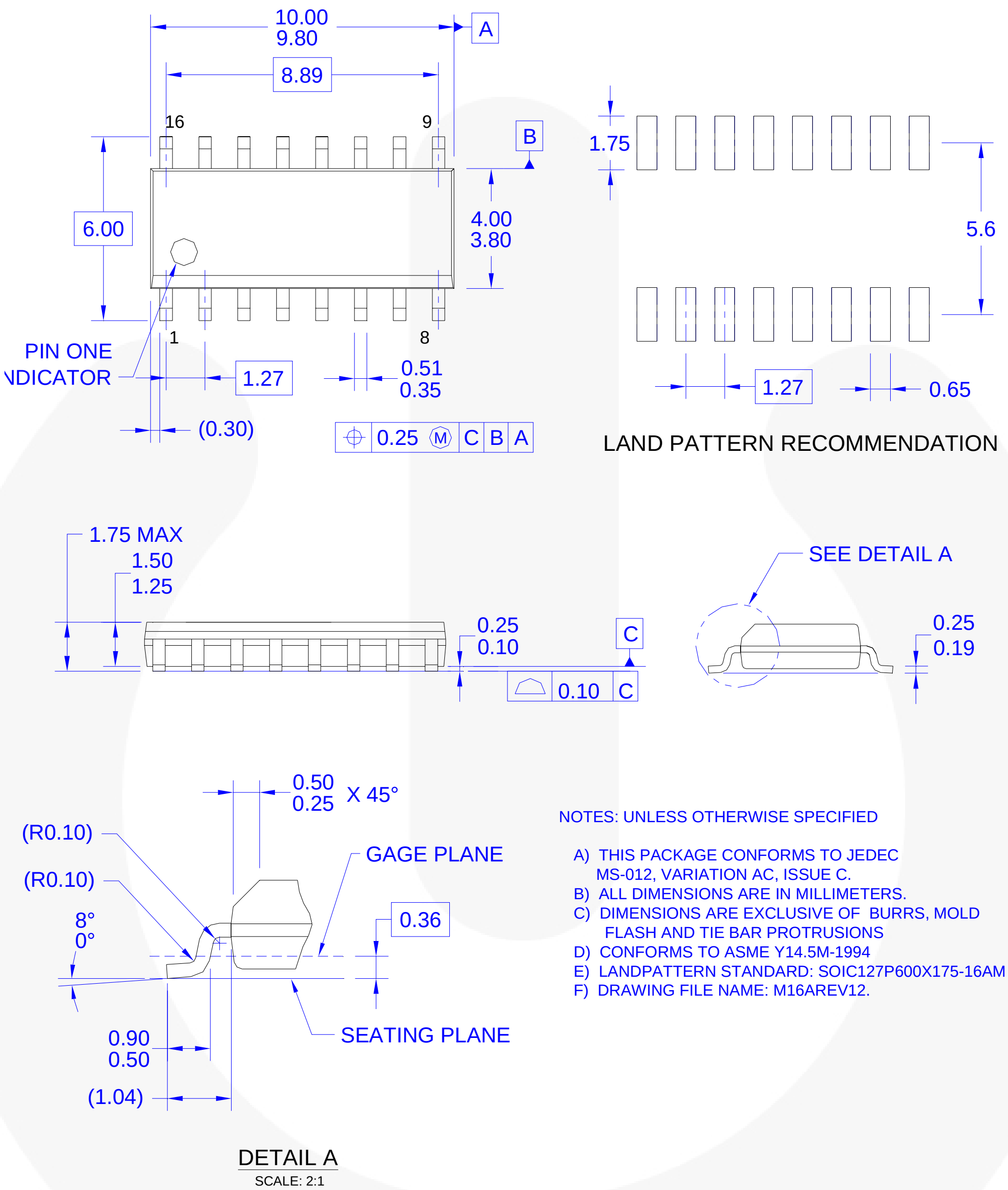

Figure 5. 16-Lead, Small Outline Integrated Circuit (SOIC)

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Physical Dimensions

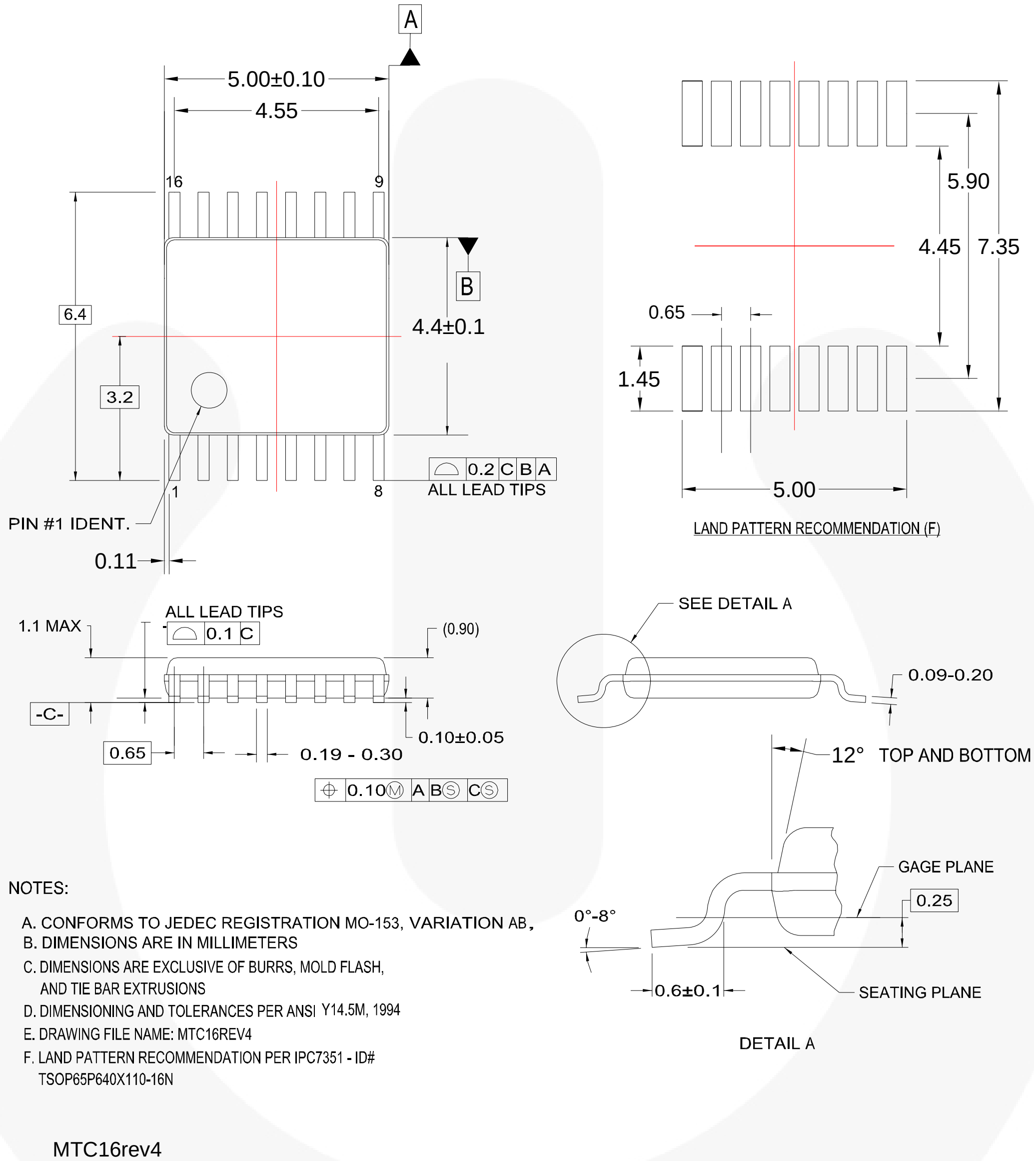

Figure 6. 16-Lead Thin Shrink Small Outline Package (TSSOP)

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Physical Dimensions

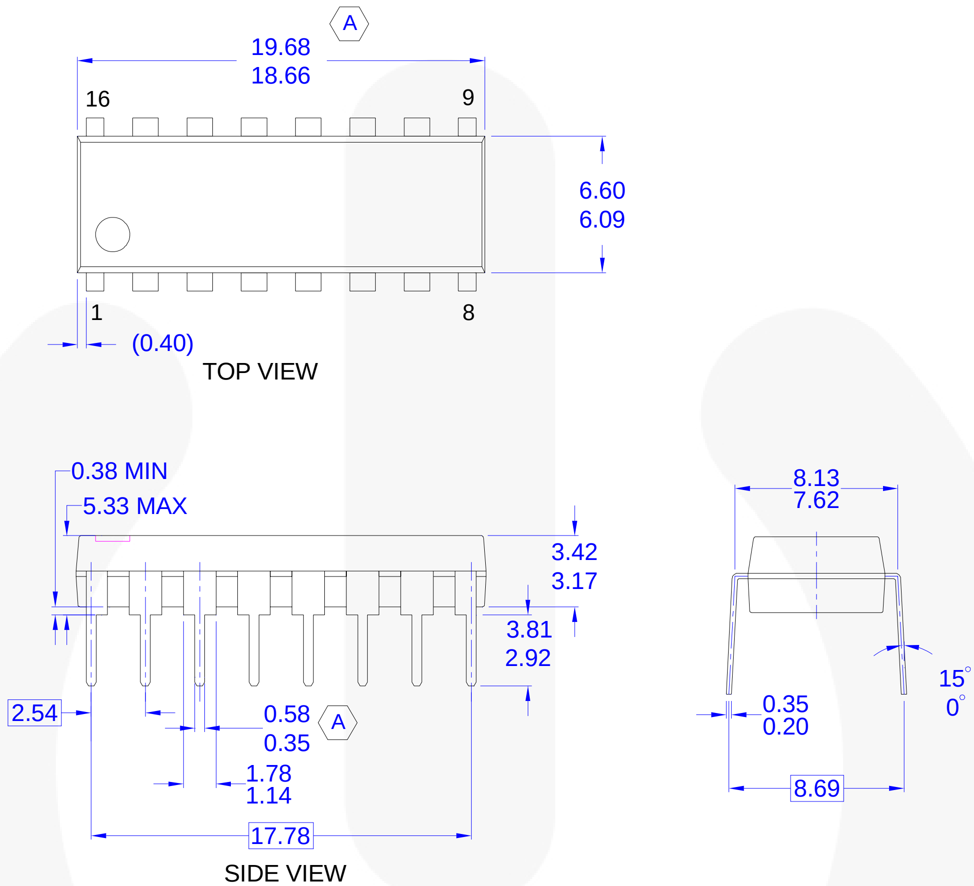

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Figure 7. 16-Lead Plastic Dual-In-Line Package (PDIP)

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